A CCD Experimental platform for large telescope in Antarctica based on FPGA

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ABSTRACT

The CCD , as a detector , is one of the important components of astronomical telescopes. For a large telescope in Antarctica, a set of CCD detector system with large size, high sensitivity and low noise is indispensable. Because of the extremely low temperatures and unattended, system maintenance and software and hardware upgrade become hard problems. This paper introduces a general CCD controller experiment platform, using Field programmable gate array FPGA, which is, in fact, a large-scale field reconfigurable array. Taking the advantage of convenience to modify the system, construction of driving circuit, digital signal processing module, network communication interface, control algorithm validation, and remote reconfigurable module may realize. With the concept of integrated hardware and software, the paper discusses the key technology of building scientific CCD system suitable for the special work environment in Antarctica, focusing on the method of remote reconfiguration for controller via network and then offering a feasible hardware and software solution.

Keywords: FPGA, a general CCD controller experiment platform, remote reconfiguration , hardware and software solution

1. INTRODUCTION

Charge coupled device as the photoelectric image sensor with high performance, has been widely used in astronomical instruments. Since the beginning of 2006, the researchers at our institute began to develop the Antarctic astronomical instruments. The Antarctic Observatory project is now being applied, and will use multi components CCD array camera, so the experiment platform need to be built for learning some key technologies of constructing CCD controller, and verifying some predictive operation at low temperature .

A CCD system includes a lot of electronic circuit, data acquisition technology and computer technology. Development of large scale integrated circuit and computer technology, has greatly simplified the production of control system. Even so,

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adjusting it to normal work is still not an easy job. A scientific CCD system consists of two pieces of hardware and software. Figure1 is a typical CCD schematic diagram.

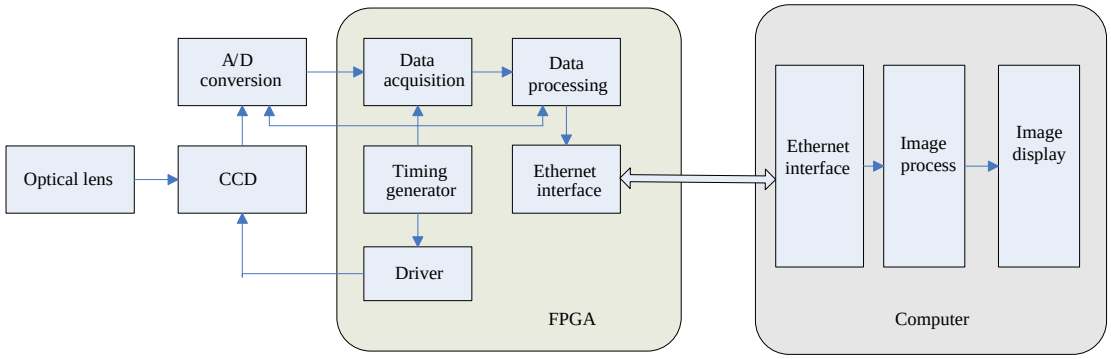

Fig.1. A typical CCD control system schematic diagram

The CCD controller mainly includes driving circuit, analog signal preprocessing circuit, analog digital converter and computer interface module. The light of objects comes to the sensitive region of the CCD through the optical system, Each pixel in CCD produces charge signal as per different intensity of light and output subsequently to AD conversion circuit. The digital signal feeds into the FPGA . FPGA is the key to generate drive signals, driving CCD for normal work，and driving shaping amplifier , analog digital conversion and so on.

2. THE HARDWARE OF PLATFORM

Using the programmable logic device driver of CCD array has become a large number of scientific developers' consensus, we have developed FPGA controller successfully as the hardware platform, generating module, network communication interface, remote reconstruction technique in the above test driver.

We select commercial EP3C40F484C6 kernel board bought in the Chinese market as the main control board, which coupled with our own extensions board to make up the hardware of platform. The kernel board is based on ALTERA Cyclone III family EP3C40F484C6 chip, including: 50MHz active crystals, JTAG download port, 16MB high-speed Flash memory (used to store configuration files and software code, etc.), 1MB off-chip SRAM, 32M × 16 DDR2 SDRAM memory, Reset Button, LED, and so on.

Meanwhile, the hardware of platform needs to design Ethernet communication module for connecting with the host computer. A DP83848C Ethernet controller chip which is based on MegaCore function of Altera's Triple-speed Ethernet, is installed in the extension board. Extension board includes the voltage conversion module, network communication module, and two DB9 COM ports to communicate with the host computer. In the HW & SW the Design stage of FPGA design, a SOPC system have to be built first using Quartus II software (including IP cores: the NIOS II processor, Triple the Speed the Ethernet, the PIO, DDR2, and the SRAM, etc), in which the Triple the Speed Ethernet core communicate with external 10/100 Mb / s MAC, A large number of PIOs are connected to terminals. After the hardware design is complete, the design control software can be completed with the help of ALTERA NIOS II the EDS.

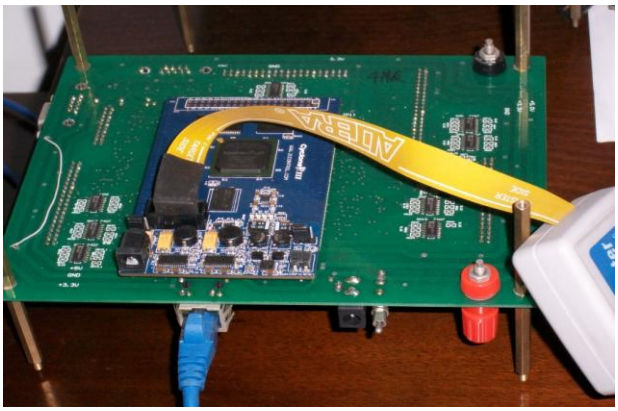

Fig.2. The Prototype of EP3C40F484C6-based FPGA kernel board

3. DRIVING TIME SEQUENCE GENERATION MODULE

Driving circuit is to ensure all required pulses for CCD, such as row, column drive pulses, the output amplifier reset pulse etc. Often also generated are the analog processing , analog to digital converter control pulse needed behind. These pulses are phase coordinated strictly. The error will be caused by the disturbance of each point in the whole system. Even the back edge of the pulse rate should also be taken care of, neither too slow, and nor too steep. Driving pulses for different chips are different greatly, ought to fitting to the given data in product specification. As possible Timing can be divided into frame timing, line transfer timing and pixel readout timing. The charge signals are finally readout in sequence from shift registers pixel by pixel.

Because of the complexity of area array CCD camera driver, we use hardware description language Verilog to design of CCD timing, which have strong ability for system hardware description and system simulation with the design method from top to down. For design of complex CCD driving timing generator, the key is how to describe the driving relationship with Verilog language. Driving sequence specification can have a variety of ways. Among them, state diagram method is simple and clear. All the possible states must be rowed, then clear logic states, programming and simulation with Verilog. State diagram is shown in figure3, while waveform diagram in figure4.

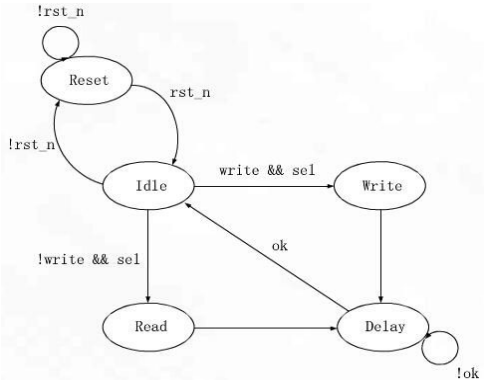

Fig.3. Driving sequence state diagram

The experimental platform is versatile and flexible, so software and hardware developed on it have flexible transfer performance and can implement different clock timing sequence by modifying hardware description language.

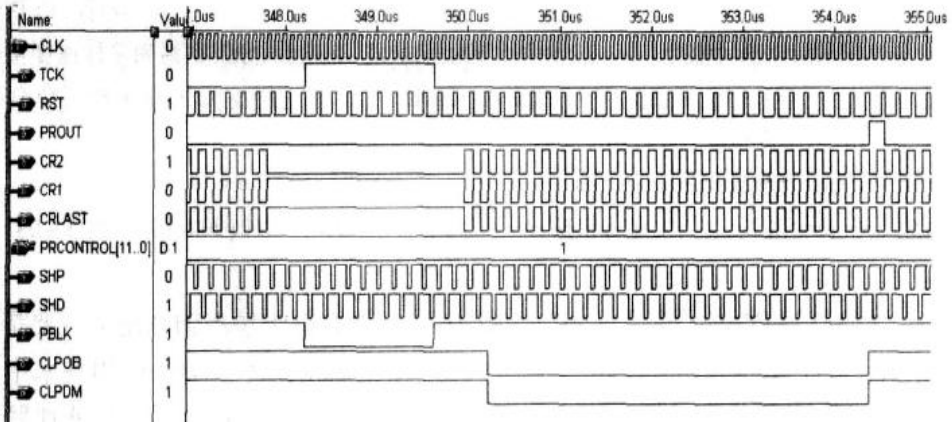

Fig.4. Timing sequence simulation waveform diagram

4. THE NETWORK COMMUNICATION INTERFACE

Large amounts of image data collected and processed by FPGA need to be transmitted to the computer for further processing, display and storage. In order to fast and long-distance transmission of data, ethernet communication interface is constructed on the experimental platform, so as to realize communication between FPGA and computer with the TFTP (Trivial File Transfer Protocol) protocol.

4. 1 Transport server

TFTP is a lightweight file transfer protocol. Any transport starts at a request of reading file or writing file. The request is also a connection request. If the server approves the request, the server opens the connection. The data transfer with fixed-length 512-byte. Each data packet contains a block of data. Server must get a customer's confirmation of the last data package before sending the next one. If a packet size of less than 512 bytes, the transferred packet is structure. If the packet is lost during transmission, sender will resend the last one data packet which have not been confirmed, when time is over. Both sides of communication are sender and receiver. That is, to send data and to receive responses on one side,while to send response and to receive data on the other side.

Transmitting on the Internet, use TFTP packets with a common header format as follows:

| Local Medium | Internet | Datagram | TFTP |

They are local medium header, IP header, the data header, TFTP header respectively, and the remaining is the TFTP data. TFTP header consists of two byte opcodes. These codes define the type of packet. There are 5 types. The packet format for data transmission is as follows:

| Operate code （ 3 byte) |Packet number | data |

TFTP is based on TCP or UDP protocols. In order to be compatible with control instruction set and easy to extend to the TFTP as well, the design is realized with UDP protocol.

4.2 Expansion server

To reduce the complexity of the software, the system control commands are put in UDP packets and transmitted to the

TFTP processor, therefore, the TFTP protocol processor on FPGA should be able to filter out non-TFTP packets and hand them to other processors, Because the first two bytes of TFTP packets define the packet content type, so those, not belong to TFTP protocol packets, can be resolved out to deal with through other paths.

In addition, the server may also achieve FLASH write function, so that when receiving the data, those data are, at the same time, written to configuration library. FLASH writing must rely on the related IP core which is associated with hardware design: flash_ssram_tristate_bridge and flash_ssram_pipeline_bridge. Corresponding to the IP cores, system software will generate a corresponding interface of software operation: alt_write_flash_block () .By this interface, you can write data to FLASH.

4. 3 Restart flow

Corresponding to REMOTE_UPDATE IP cores, there are a group of macro commands in system software:Altremote_Update Megafunction. It is a user- friendly interface for operation control registers and status registers in software.

With the above hardware and software design, you can complete selection loading process for configuration library as follows:

1) Write the address of next start configuration to control register.

2) May use the watchdog circuit in configuration.

3) Set the period of running the watchdog in configuration.

4) Read status register, decided the cause of reopen, helping to make decision.

5) Trigger upgrade circuit. Reconfigurate FPGA with a specified configuration.

The key program to achieve the above procedures is as follows:

```
void reconfig_fpga(int hw_flash_offset) // hw_flash_offset set the address for restart
{
volatile int remote_update_base;
remote_update_base = REMOTE_UPDATE_BASE;
IOWR_16DIRECT( EXT_FLASH_BASE, 0, 0xFFFF );
IOWR_8DIRECT( EXT_FLASH_BASE, 0, 0xFF );
IOWR( remote_update_base, 0x3, 0 );
IOWR( remote_update_base, 0x4, hw_flash_offset >> 3 );
IOWR( remote_update_base, 0x20, 0x1 );
while( 1 );
return;
}
```

Fig.5. The operation interface of Remote reconfiguration

4. 4 Remote reconfiguration

If the Internet is smooth, by using the FPGA remote reconfiguration technology, a CCD controller can be upgraded reconstruction in anywhere of the world.

Firstly, to compile the project updated, generate a new flash file, downloading to the FPGA chip by TFTP protocol and Ethernet Remote, then sending "reconfig" to restart FPGA. Figure5 is operation interface of Remote reconfiguration.

5. RESULTS AND IMPROVEMENTS

The work presented in this paper started as a request for Antarctic CCD controller study, with the aim to familiar with FPGA hardware platform, driving time sequence generation, network communication interface , remote reconfiguration and so on. Under the ALTERA complete development and testing environments and local area network conditions, by actual verification and testing, this design proves reliable, meeting the actual demands of key technology for building scientific CCD system. Due to the structure of the driving circuit being programmable, without changing any hardware, only need to reprogramming device, the driving circuit can be updated easily. In the case that LAN is connected to ethernet , you can also remotely upgrade off-site via INTENET. It provides a strong support in operation and remote maintenance for large-scale systems.

ACKNOWLEDGMENTS

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