Design and realization of the IP control core in field controllers for LAMOST spectroscopes[1]

Jianing Wang[ab2], Zhongyi Han[abc], Yizhong Zeng[ab], Songxin Dai[ab], Zhongwen Hu[ab], Yongtian Zhu[ab], Lei Wang[ab], Yonghui Hou[ab]

a. National Astronomical Observatories / Nanjing Institute of Astronomical Optics & Technology, Chinese Academy of Sciences, Nanjing 210042, China;

b. Key Laboratory of Astronomical Optics & Technology, Nanjing Institute of Astronomical Optics & Technology, Chinese Academy of Sciences, Nanjing 210042, China;

c. Graduate University of Chinese Academy of Sciences, Beijing 100049, China

ABSTRACT

The China-made telescope, LAMOST, consists of 16 spectroscopes to detect stellar spectra via 4000 optical fibers. In each spectroscope, many movable parts work in phase. Those parts are real-time controlled and managed by field controllers based on FPGA. This paper mainly introduces how to use DSP Builder module library in MATLAB / Simulink to construct the IP control core on FPGA chip. This method can also be used to design the control core of PID arithmetic, to carry out arithmetic simulation and generate VHDL language file, as well as to integrate it into SOPC developing environment so as to repeatedly use. In this way, the design period of the control system may be shortened and design process simplified. Finally due to the reversibility and programmability of the IP control core ,a system on a chip for field controllers of spectroscope is realized, which meets astronomical control requirements, providing an effective scheme for embedded system in astronomical instrument applications.

Keywords: LAMOST ,field controllers, DSP Builder , IP control core , Field Programmable Gate Array (FPGA), spectroscopes, MATLAB / Simulink

1. INTRODUCTION

The control system is an important part of large astronomical telescopes. The objects to be controlled include the azimuth axis, the altitude axis, focal plane instruments, the dome and so on, so as to trace are position the observed celestial bodies. From the automation point of view, it is a servo system, composed of an open-loop control system and a closed-loop control system. The closed-loop control system works as such that fetching the feedback from controlled objects, comparing with the reference, and then adjusting the output as per a control algorithm. The earliest developed is strategy PID (Proportional, integral, differential). Its advantages are simple algorithm, good robustness and high reliability, so PID is extensively used in industrial processes control. It is also widely applied in the astronomical telescopes. Control system is typically carried out with computer, plus motor motion control cards. Such systems have powerful control ability and are easy to use, but the weakness is relatively expensive and large size, not suitable for multi-nodes and distributed control objects.

In recent years, with the rapid development of microelectronics technology, the integrated circuit design and technological level have been greatly improved, enabling to integrate an electronic system to a single silicon chip, which previously must be formed by a number of integrated circuit. This is so-called SOC (System 0n a Chip). At the same time, it promotes the active development of corresponding EDA (Electronic Design Automation) tools. FPGA (Field Programmable Gate Array) is a large-scale system on a chip. In this work author intends to use a new type of EDA tool to package PID control algorithm as a dedicated IP(Intellectual Property) core, then integrating it into the FPGA

[1] Supported by LAMOST project and National Natural Science Foundation project Distributed astronomical instrument control technology based on system on chip (NO. 10778722)

[2] Correspondence: Email: jnwang@niaot.ac.cn; Telephone: 86 25 8548 2224

Software and Cyberinfrastructure for Astronomy, edited by Nicole M. Radziwill, Alan Bridger,
Proc. of SPIE Vol. 7740, 77402N · © 2010 SPIE · CCC code: 0277-786X/10/$18 · doi: 10.1117/12.856649

development environment, so that the classic control algorithm can be adapted to the field controller of astronomical instruments through SOC.

2. FUNDAMENTAL CONTROL PRINCIPLE

PID control is in a control manner with the most mature technology, and widely used in control system. The basic principle is based on proportional, integral, differential operation of the deviation fed back from the control system. The results obtained are sent to the implementing actuators. Accordingly the implementing actuators control the controlled object.

In the continuous time domain, PID controller algorithm may be expressed as follows:

$$u = k_p\left(e + \frac{1}{T_i}\int e dt + T_d \frac{de}{dt}\right) \qquad (1)$$

Where k P is proportional gain, Ti is integration time, Td is time differential, u is control output and e is error signal.

The discrete PID control algorithm in computer can be introduced by continuous PID control algorithm. For discrete situation, differential equation (1) should be rewritten as a differential equation.

$$u(n) = k_p\left\{e(n) + \frac{T}{T_i}\sum_{j=0}^{n} e(j) + \frac{T_d}{T}\left[e(n) - e(n-1)\right]\right\} \qquad (2)$$

Where, T is sampling period, n is sample number, (n = 0,1,2,3 ...), e (n - 1) and e (n) is the error signal obtained in no. n – 1 sample and in no. n sample respectively, and u (n) is the control output of no.n sample.

Telescope control systems generally use three-loop cascade control structure, that is, current loop, velocity loop and position loop, where each loop has a PID controller. Due to the differences in the telescope mechanical structure , it is somewhat difficult to write an accurate mathematical model for all telescope control systems. This article focuses on the method which uses EDA tools to construct IP core, rather than on the analysis of motion law for telescopes, therefore uses a simple first-order system simulation for of controlled objects to emulate . Figure 1 is a block diagram of PID control system, in which PID sub-system block diagram is the design and simulation using DSP Builder.

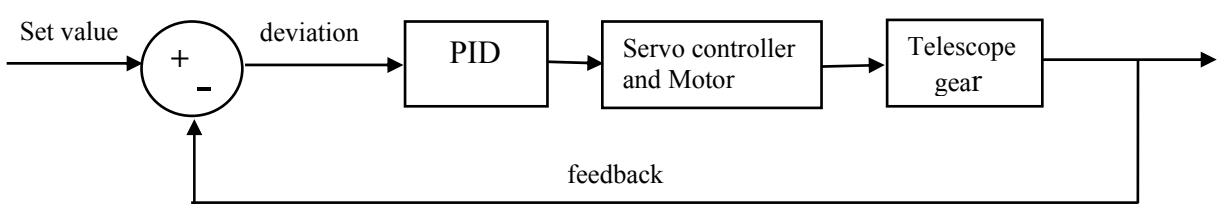

Fig.1. The block diagram of PID control system

3. USING THE DSP BUILDER COMPONENT TO BUILD PID IP CORE

For applications of system development with FPGA, there have been new design tools and design flows. Altera's DSP Builder is a system-level development tool for DSP-oriented chips .lt provides interface for development tools Quartus ® II and MATLAB / Simulink ,coming out as a Simulink as a toolbox in Matlab, which enables FPGA design of dedicated chip systems carried out by Simulink graphical interface, i.e. simply invoking the modules in DSP Builder toolbox. The basic modules in DSP Builder are of algorithm-level description, easy to be treated in system or algorithmic level by the users. The DSP Builder Signal Compiler block reads Simulink Model Files (mdl) that are built using DSP Builder and MegaCore® blocks, then creates VHDL files and tool command language (Tcl) scripts for synthesis, hardware implementation, and simulation.

3.1 PID IP control core

The controller in this paper is a position-PID controller. The design begins on system-level, without relation to hardware at all. Using Matlab's system design, analysis capabilities and DSP Builder modules, we complete control system structure design first and structure a model in Simulink. In order to generate the HDL file and write it into the FPGA , in the top-level algorithm design in Simulink, PID algorithm part is designed with DSP Builder modules. In the design process, in order to avoid floating-point computing, the PID coefficients are taken as integer and amplified them as 24-bit data. After the parallel adder computing unit, with the bus converter module, the accumulated data are bits converted, indirectly implementing the floating-point operations in FPGA. Figure 2 is a block diagram of PID control algorithm. In the diagram, algorithm itself is inside the dashed block, which can be implemented in the FPGA. Other parts of the components are common Simulink modules for simulation use.

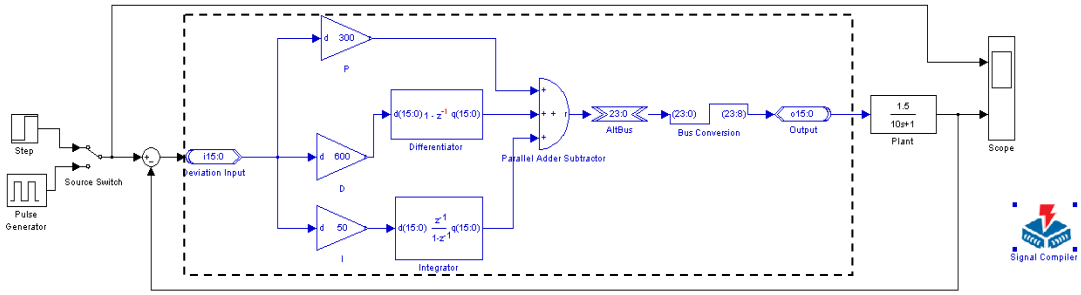

Fig.2. The block diagram of PID control algorithm

A first-order system emulated with the controlled object is set up for simulation in this paper. Signal generator gives system settings here with the rectangular wave and step signal to emulate the system settings. Figure 3 is a step signal and square wave signals in Simulink emulated results.

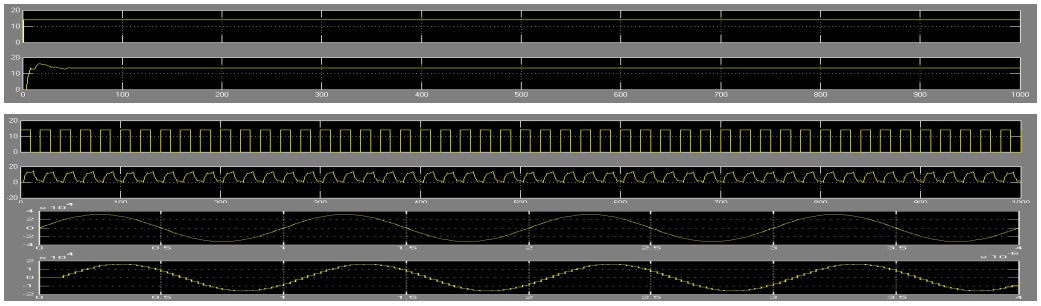

Fig.3. A step signal , square wave and sine wave in Simulink emulated results

In order to transfer the graphical top-level design models in Simulink to HDL language description files which are identifiable for FPGA development software, we have ordered a DSP Builder software license from ALTERA. Opening the Signal compiler modules and configurating the relative parameters,"PID control algorithm" designed with DSP Builder can be compiled as modules described VHDL and Veirlog language and tool command language Tcl scripts. According to the compilation of the previous design model, the tb_PID.tcl feature simulation files scripts for access to ModelSim and the project files tb_PID.qpf required for Quartus are also obtained.
After opening the file tb_PID.tcl in the ModelSim menu and debugging successfully, the simulation results is as Figure 4. Functional simulation results are basically consistent with that in Matlab, basically proving the success of top-level design.

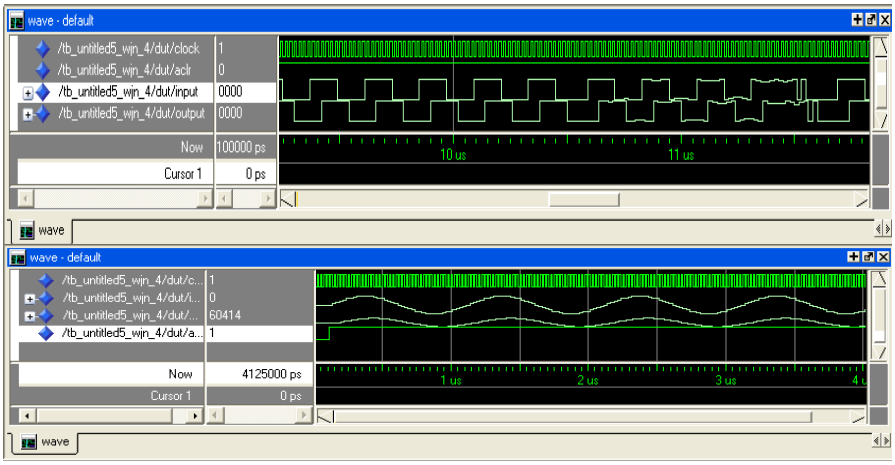

Fig.4. Simulation results of square wave and a sine wave in ModelSim

The PID module's input and output, coupled with Avalon-MM Slave interface, can be integrated in the SOPC Builder development environment, to form a PID control IP core and be repeatedly called. Figure 5 is a PID's control IP in the left side of the module table, after adding to the SOPC Builder development environment. It will be added to the SOPC system which is under construction.

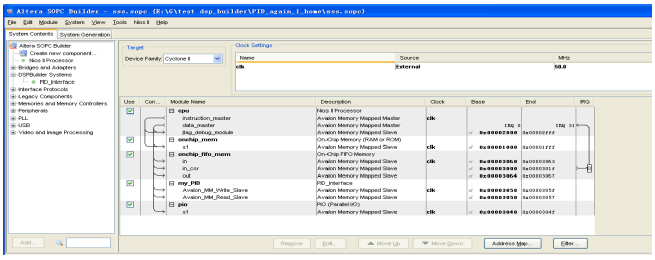

Fig.5. SOPC system after adding PID IP core

Combining the bus interface, a variety of necessary peripheral components, flash, PIO and so on, compile the SOPC system and download it to the FPGA. To facilitate programming, we may also set the PID hardware modules as corresponding instructions through SOPC Builder development environment and call them with control programs. In this way, not only hardware modules may run with a relatively rapid speed, but also keep the flexibility of software control.

3.2 IP control core of optical encoder

Another important components in astronomical control systems are position detection devices which are usually optical encoders. Optical encoder is a rotary position sensor. They are widely used in angular displacement or angular rate measurement in modern servo systems. Its axis is usually connected to the measured rotation axis and rotates

synchronously with the measured axis. Angular displacement can be converted to a string of binary codes pulses. Optical encoder is divided into two types , absolute encoder and incremental encoder. Incremental optical encoders have many advantages, such as simple structure, small size, low price, high precision, fast response, stable performance etc, so widely used in astronomical instrument control systems.

Incremental encoder gives a string of pulses when rotating. A counter adds or subtracts these pulses according to direction of rotation, giving out the angular displacement of rotation axis. Coaxial installed optical encoder will output A B two digital pulse signals with 90° phase difference as the detection object spinning. When the optical encoder clockwise rotates, the channel A outputs waveforms leading the channel B output waveforms 90°. Likewise when the optical encoder counterclockwise rotates, the channel A outputs waveforms delaying the channel B waveforms 90°. The output waveform of optical encoder is shown in Figure 6.

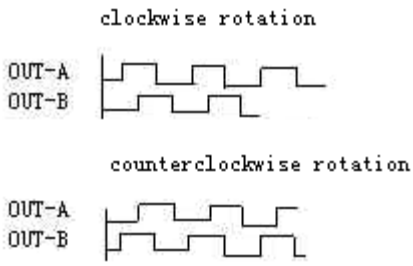

Fig.6. The output waveform of optical encoder

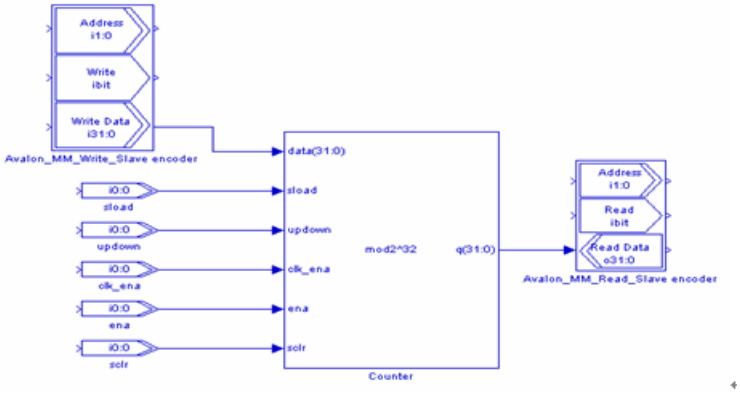

Fig.7. Bidirectional count circuit

A phase discrimination and bidirectional count circuit is needed to separate the signals from encoder to obtain the rotating position. A bidirectional count circuit model, coupled with Avalon-MM Slave interface, can be integrated in the SOPC Builder development environment, to form an encoder control IP core and be repeatedly called. Bidirectional count circuit is shown in Figure 7.

To construct the phase discrimination circuit of encoder, a D flip-flop circuit is needed, but it cannot be find in DSP Builder toolbox. Therefore a D flip-flop is added to project built by Quartus development. The output pin Q of D flip-flop is connected to the updown pin of bidirectional counter. The pulses output pin of encoder A is connected to the sload pin of bidirectional counter. When the optical encoder clockwise rotates, the channel A outputs waveforms leading channel B output waveforms 90°. The output pin Q of D flip-flop is high.The bidirectional count circuit adds the counter according to pulses of sload pin. When the optical encoder counterclockwise rotates, the channel A outputs waveforms delaying the channel B outputs waveforms 90°. The output pin Q of D flip-flop is low. The bidirectional count circuit subtracts the counter according to pulses of sload pin. Encoder counter is read from the Avalon bus and converted into angular position value by NIOS CPU. Encoder interface module implemented in the Quartus is shown in Figure 8.

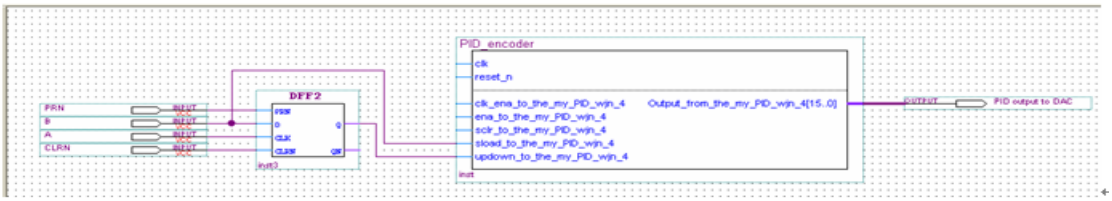

Fig.8. Encoder interface module

4. PRELIMINARY CONCLUSIONS AND FUTURE WORK

We use LAMOST spectrometer on-site controller as the hardware development platform. The on-site controller hardware of panels is composed of ALTERA's FPGA CycloneII devices. Its basic configurations are: Cyclone Ⅱ EP2C35F672C6ES FPGA, SRAM 2MB, Flash 16MB, Dual tolerant 5V inputs extended port, 2 * 41 I / O, MAX ® EPM256AE CPLD control logic, EPCS64 FPGA serial configuration chip, Ethernet interface (RJ45), serial port (RS232 DB9) and so on. These function blocks are integrated into an FPGA chip, forming a programmable system on a chip system (SOPC). Burning it into a FPGA circuit, the hardware design of on-site controller for spectrometer is completed. Coupled with self-designed PID IP and encoder interface module for control motor movements and the DC motor, a closed-loop control circuit is formed. Control software block diagram is shown in Figure 9

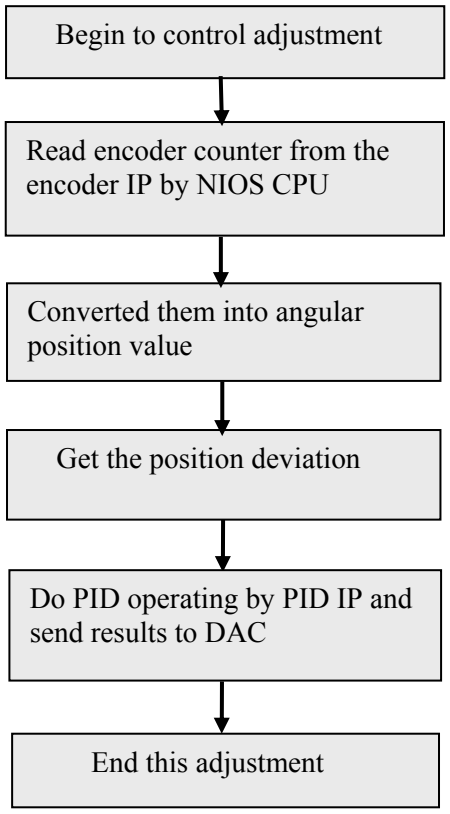

Fig.9. The Control software block diagram of PID system

The design process above indicates that using DSP Builder blocks in MATLAB / Simulink library for control system modeling, may help the conventional engineers quickly applying the idea of the algorithm-level design conception to control system design, which may save them limited energy for system-level algorithm design since it avoids many complicated and time-consuming circuit designs and shortens the time period from conception to the realization. A complex electronic system designs may be achieved simply by setting up the basic parameters of each module in DSP Builder library, without having to understand the concrete process of realization for each module in detail. And more, even you may get rid of the knowledge of FPGA itself and hardware description language. True electronic system design of the black box, building blocks and simplification is eventually possible. We are trying to assemble more relative control module as IP cores through the DSP Builder so as to quickly construct an astronomical instrument control system in FPGA, then making the reconstruction or updating for hardware and software more easy in the astronomical Instruments.

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